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;Supported Devices:

; EFM8SB10F2G

; EFM8SB10F4G

; EFM8SB10F8G

; EFM8SB10F8G

; EFM8SB10F8G

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; Register Definitions

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ACC DATA 0E0H; Accumulator

ADC0AC DATA 0BAH; ADC0 Accumulator Configuration

ADC0CF DATA 097H; ADC0 Configuration

ADC0CN0 DATA 0E8H; ADC0 Control 0

ADC0GTH DATA 0C4H; ADC0 Greater-Than High Byte

ADC0GTL DATA 0C3H; ADC0 Greater-Than Low Byte

ADC0H DATA 0BEH; ADC0 Data Word High Byte

ADC0L DATA 0BDH; ADC0 Data Word Low Byte

ADC0LTH DATA 0C6H; ADC0 Less-Than High Byte

ADC0LTL DATA 0C5H; ADC0 Less-Than Low Byte

ADC0MX DATA 096H; ADC0 Multiplexer Selection

ADC0PWR DATA 0BBH; ADC0 Power Control

ADC0TK DATA 0BCH; ADC0 Burst Mode Track Time

B DATA 0F0H; B Register

CKCON0 DATA 08EH; Clock Control 0

CLKSEL DATA 0A9H; Clock Select

CMP0CN0 DATA 09BH; Comparator 0 Control 0

CMP0MD DATA 09DH; Comparator 0 Mode

CMP0MX DATA 09FH; Comparator 0 Multiplexer Selection

CRC0AUTO DATA 09EH; CRC0 Automatic Control

CRC0CN0 DATA 084H; CRC0 Control 0

CRC0CNT DATA 09AH; CRC0 Automatic Flash Sector Count

CRC0DAT DATA 086H; CRC0 Data Output

CRC0FLIP DATA 09CH; CRC0 Bit Flip

CRC0IN DATA 085H; CRC0 Data Input

CS0CF DATA 0AAH; Capacitive Sense 0 Configuration

CS0CN0 DATA 0B0H; Capacitive Sense 0 Control

CS0DH DATA 0EEH; Capacitive Sense 0 Data High Byte

CS0DL DATA 0EDH; Capacitive Sense 0 Data Low Byte

CS0MD1 DATA 0AFH; Capacitive Sense 0 Mode 1

CS0MD2 DATA 0F3H; Capacitive Sense 0 Mode 2

CS0MD3 DATA 0F3H; Capacitive Sense 0 Mode 3

CS0MX DATA 0ABH; Capacitive Sense 0 Mux Channel Select

CS0PM DATA 0DEH; Capacitive Sense 0 Pin Monitor

CS0SCAN0 DATA 0D2H; Capacitive Sense 0 Channel Scan Mask 0

CS0SCAN1 DATA 0D3H; Capacitive Sense 0 Channel Scan Mask 1

CS0SE DATA 0DEH; Capacitive Sense 0 Auto Scan End Channel

CS0SS DATA 0DDH; Capacitive Sense 0 Auto Scan Start Channel

CS0THH DATA 0FEH; Capacitive Sense 0 Comparator Threshold High Byte

CS0THL DATA 0FDH; Capacitive Sense 0 Comparator Threshold Low Byte

DERIVID DATA 0E3H; Device Identification

DPH DATA 083H; Data Pointer High

DPL DATA 082H; Data Pointer Low

EIE1 DATA 0E6H; Extended Interrupt Enable 1

EIE2 DATA 0E7H; Extended Interrupt Enable 2

EIP1 DATA 0F6H; Extended Interrupt Priority 1

EIP2 DATA 0F7H; Extended Interrupt Priority 2

FLKEY DATA 0B7H; Flash Lock and Key

FLSCL DATA 0B6H; Flash Scale

HFO0CAL DATA 0B3H; High Frequency Oscillator Calibration

HFO0CN DATA 0B2H; High Frequency Oscillator Control

IE DATA 0A8H; Interrupt Enable

IP DATA 0B8H; Interrupt Priority

IREF0CF DATA 0B9H; Current Reference Configuration

IREF0CN0 DATA 0D6H; Current Reference Control 0

IT01CF DATA 0E4H; INT0/INT1 Configuration

P0 DATA 080H; Port 0 Pin Latch

P0DRV DATA 099H; Port 0 Drive Strength

P0MASK DATA 0C7H; Port 0 Mask

P0MAT DATA 0D7H; Port 0 Match

P0MDIN DATA 0F1H; Port 0 Input Mode

P0MDOUT DATA 0A4H; Port 0 Output Mode

P0SKIP DATA 0D4H; Port 0 Skip

P1 DATA 090H; Port 1 Pin Latch

P1DRV DATA 09BH; Port 1 Drive Strength

P1MASK DATA 0BFH; Port 1 Mask

P1MAT DATA 0CFH; Port 1 Match

P1MDIN DATA 0F2H; Port 1 Input Mode

P1MDOUT DATA 0A5H; Port 1 Output Mode

P1SKIP DATA 0D5H; Port 1 Skip

P2 DATA 0A0H; Port 2 Pin Latch

P2DRV DATA 09DH; Port 2 Drive Strength

P2MDOUT DATA 0A6H; Port 2 Output Mode

PCA0CN0 DATA 0D8H; PCA Control 0

PCA0CPH0 DATA 0FCH; PCA Channel 0 Capture Module High Byte

PCA0CPH1 DATA 0EAH; PCA Channel 1 Capture Module High Byte

PCA0CPH2 DATA 0ECH; PCA Channel 2 Capture Module High Byte

PCA0CPL0 DATA 0FBH; PCA Channel 0 Capture Module Low Byte

PCA0CPL1 DATA 0E9H; PCA Channel 1 Capture Module Low Byte

PCA0CPL2 DATA 0EBH; PCA Channel 2 Capture Module Low Byte

PCA0CPM0 DATA 0DAH; PCA Channel 0 Capture/Compare Mode

PCA0CPM1 DATA 0DBH; PCA Channel 1 Capture/Compare Mode

PCA0CPM2 DATA 0DCH; PCA Channel 2 Capture/Compare Mode

PCA0H DATA 0FAH; PCA Counter/Timer High Byte

PCA0L DATA 0F9H; PCA Counter/Timer Low Byte

PCA0MD DATA 0D9H; PCA Mode

PCA0PWM DATA 0DFH; PCA PWM Configuration

PCON0 DATA 087H; Power Control 0

PMU0CF DATA 0B5H; Power Management Unit Configuration

PMU0FL DATA 0CEH; Power Management Unit Flag

PMU0MD DATA 0B5H; Power Management Unit Mode

PSCTL DATA 08FH; Program Store Control

PSW DATA 0D0H; Program Status Word

REF0CN DATA 0D1H; Voltage Reference Control

REG0CN DATA 0C9H; Voltage Regulator Control

REVID DATA 0E2H; Revision Identifcation

RSTSRC DATA 0EFH; Reset Source

RTC0ADR DATA 0ACH; RTC Address

RTC0DAT DATA 0ADH; RTC Data

RTC0KEY DATA 0AEH; RTC Lock and Key

SBUF0 DATA 099H; UART0 Serial Port Data Buffer

SCON0 DATA 098H; UART0 Serial Port Control

SFRPAGE DATA 0A7H; SFR Page

SMB0ADM DATA 0F5H; SMBus 0 Slave Address Mask

SMB0ADR DATA 0F4H; SMBus 0 Slave Address

SMB0CF DATA 0C1H; SMBus 0 Configuration

SMB0CN0 DATA 0C0H; SMBus 0 Control

SMB0DAT DATA 0C2H; SMBus 0 Data

SP DATA 081H; Stack Pointer

SPI0CFG DATA 0A1H; SPI0 Configuration

SPI0CKR DATA 0A2H; SPI0 Clock Rate

SPI0CN0 DATA 0F8H; SPI0 Control

SPI0DAT DATA 0A3H; SPI0 Data

TCON DATA 088H; Timer 0/1 Control

TH0 DATA 08CH; Timer 0 High Byte

TH1 DATA 08DH; Timer 1 High Byte

TL0 DATA 08AH; Timer 0 Low Byte

TL1 DATA 08BH; Timer 1 Low Byte

TMOD DATA 089H; Timer 0/1 Mode

TMR2CN0 DATA 0C8H; Timer 2 Control 0

TMR2H DATA 0CDH; Timer 2 High Byte

TMR2L DATA 0CCH; Timer 2 Low Byte

TMR2RLH DATA 0CBH; Timer 2 Reload High Byte

TMR2RLL DATA 0CAH; Timer 2 Reload Low Byte

TMR3CN0 DATA 091H; Timer 3 Control 0

TMR3H DATA 095H; Timer 3 High Byte

TMR3L DATA 094H; Timer 3 Low Byte

TMR3RLH DATA 093H; Timer 3 Reload High Byte

TMR3RLL DATA 092H; Timer 3 Reload Low Byte

TOFFH DATA 08EH; Temperature Sensor Offset High

TOFFL DATA 08DH; Temperature Sensor Offset Low

VDM0CN DATA 0FFH; VDD Supply Monitor Control

XBR0 DATA 0E1H; Port I/O Crossbar 0

XBR1 DATA 0E2H; Port I/O Crossbar 1

XBR2 DATA 0E3H; Port I/O Crossbar 2

XOSC0CN DATA 0B1H; External Oscillator Control

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; 16-bit Register Definitions (may not work on all compilers)

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ADC0GT DATA 0C3H ; ADC0 Greater-Than Low Byte

ADC0 DATA 0BDH ; ADC0 Data Word Low Byte

ADC0LT DATA 0C5H ; ADC0 Less-Than Low Byte

DP DATA 082H ; Data Pointer Low

PCA0CP0 DATA 0FBH ; PCA Channel 0 Capture Module Low Byte

PCA0CP1 DATA 0E9H ; PCA Channel 1 Capture Module Low Byte

PCA0CP2 DATA 0EBH ; PCA Channel 2 Capture Module Low Byte

PCA0 DATA 0F9H ; PCA Counter/Timer Low Byte

TMR2 DATA 0CCH ; Timer 2 Low Byte

TMR2RL DATA 0CAH ; Timer 2 Reload Low Byte

TMR3 DATA 094H ; Timer 3 Low Byte

TMR3RL DATA 092H ; Timer 3 Reload Low Byte

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; Indirect Register Definitions

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ALARM0 EQU 008H ; RTC Alarm Programmed Value 0

ALARM1 EQU 009H ; RTC Alarm Programmed Value 1

ALARM2 EQU 00AH ; RTC Alarm Programmed Value 2

ALARM3 EQU 00BH ; RTC Alarm Programmed Value 3

CAPTURE0 EQU 000H ; RTC Timer Capture 0

CAPTURE1 EQU 001H ; RTC Timer Capture 1

CAPTURE2 EQU 002H ; RTC Timer Capture 2

CAPTURE3 EQU 003H ; RTC Timer Capture 3

RTC0CN0 EQU 004H ; RTC Control 0

RTC0XCF EQU 006H ; RTC Oscillator Configuration

RTC0XCN0 EQU 005H ; RTC Oscillator Control 0

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; Bit Definitions

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; ACC 0xE0 (Accumulator)

ACC\_ACC0 BIT ACC.0 ; Accumulator Bit 0

ACC\_ACC1 BIT ACC.1 ; Accumulator Bit 1

ACC\_ACC2 BIT ACC.2 ; Accumulator Bit 2

ACC\_ACC3 BIT ACC.3 ; Accumulator Bit 3

ACC\_ACC4 BIT ACC.4 ; Accumulator Bit 4

ACC\_ACC5 BIT ACC.5 ; Accumulator Bit 5

ACC\_ACC6 BIT ACC.6 ; Accumulator Bit 6

ACC\_ACC7 BIT ACC.7 ; Accumulator Bit 7

; ADC0CN0 0xE8 (ADC0 Control 0)

ADC0CN0\_ADCM0 BIT ADC0CN0.0 ; Start of Conversion Mode Select Bit 0

ADC0CN0\_ADCM1 BIT ADC0CN0.1 ; Start of Conversion Mode Select Bit 1

ADC0CN0\_ADCM2 BIT ADC0CN0.2 ; Start of Conversion Mode Select Bit 2

ADC0CN0\_ADWINT BIT ADC0CN0.3 ; Window Compare Interrupt Flag

ADC0CN0\_ADBUSY BIT ADC0CN0.4 ; ADC Busy

ADC0CN0\_ADINT BIT ADC0CN0.5 ; Conversion Complete Interrupt Flag

ADC0CN0\_ADBMEN BIT ADC0CN0.6 ; Burst Mode Enable

ADC0CN0\_ADEN BIT ADC0CN0.7 ; ADC Enable

; B 0xF0 (B Register)

B\_B0 BIT B.0 ; B Register Bit 0

B\_B1 BIT B.1 ; B Register Bit 1

B\_B2 BIT B.2 ; B Register Bit 2

B\_B3 BIT B.3 ; B Register Bit 3

B\_B4 BIT B.4 ; B Register Bit 4

B\_B5 BIT B.5 ; B Register Bit 5

B\_B6 BIT B.6 ; B Register Bit 6

B\_B7 BIT B.7 ; B Register Bit 7

; CS0CN0 0xB0 (Capacitive Sense 0 Control)

CS0CN0\_CSCMPF BIT CS0CN0.0 ; CS0 Digital Comparator Interrupt Flag

CS0CN0\_CSPME BIT CS0CN0.1 ; CS0 Pin Monitor Event

CS0CN0\_CSCMPEN BIT CS0CN0.3 ; CS0 Digital Comparator Enable

CS0CN0\_CSBUSY BIT CS0CN0.4 ; CS0 Busy

CS0CN0\_CSINT BIT CS0CN0.5 ; CS0 Interrupt Flag

CS0CN0\_CSEOS BIT CS0CN0.6 ; CS0 End of Scan Interrupt Flag

CS0CN0\_CSEN BIT CS0CN0.7 ; CS0 Enable

; IE 0xA8 (Interrupt Enable)

IE\_EX0 BIT IE.0 ; External Interrupt 0 Enable

IE\_ET0 BIT IE.1 ; Timer 0 Interrupt Enable

IE\_EX1 BIT IE.2 ; External Interrupt 1 Enable

IE\_ET1 BIT IE.3 ; Timer 1 Interrupt Enable

IE\_ES0 BIT IE.4 ; UART0 Interrupt Enable

IE\_ET2 BIT IE.5 ; Timer 2 Interrupt Enable

IE\_ESPI0 BIT IE.6 ; SPI0 Interrupt Enable

IE\_EA BIT IE.7 ; All Interrupts Enable

; IP 0xB8 (Interrupt Priority)

IP\_PX0 BIT IP.0 ; External Interrupt 0 Priority Control

IP\_PT0 BIT IP.1 ; Timer 0 Interrupt Priority Control

IP\_PX1 BIT IP.2 ; External Interrupt 1 Priority Control

IP\_PT1 BIT IP.3 ; Timer 1 Interrupt Priority Control

IP\_PS0 BIT IP.4 ; UART0 Interrupt Priority Control

IP\_PT2 BIT IP.5 ; Timer 2 Interrupt Priority Control

IP\_PSPI0 BIT IP.6 ; Serial Peripheral Interface (SPI0) Interrupt Priority Control

; P0 0x80 (Port 0 Pin Latch)

P0\_B0 BIT P0.0 ; Port 0 Bit 0 Latch

P0\_B1 BIT P0.1 ; Port 0 Bit 1 Latch

P0\_B2 BIT P0.2 ; Port 0 Bit 2 Latch

P0\_B3 BIT P0.3 ; Port 0 Bit 3 Latch

P0\_B4 BIT P0.4 ; Port 0 Bit 4 Latch

P0\_B5 BIT P0.5 ; Port 0 Bit 5 Latch

P0\_B6 BIT P0.6 ; Port 0 Bit 6 Latch

P0\_B7 BIT P0.7 ; Port 0 Bit 7 Latch

; P1 0x90 (Port 1 Pin Latch)

P1\_B0 BIT P1.0 ; Port 1 Bit 0 Latch

P1\_B1 BIT P1.1 ; Port 1 Bit 1 Latch

P1\_B2 BIT P1.2 ; Port 1 Bit 2 Latch

P1\_B3 BIT P1.3 ; Port 1 Bit 3 Latch

P1\_B4 BIT P1.4 ; Port 1 Bit 4 Latch

P1\_B5 BIT P1.5 ; Port 1 Bit 5 Latch

P1\_B6 BIT P1.6 ; Port 1 Bit 6 Latch

P1\_B7 BIT P1.7 ; Port 1 Bit 7 Latch

; P2 0xA0 (Port 2 Pin Latch)

P2\_B7 BIT P2.7 ; Port 2 Bit 7 Latch

; PCA0CN0 0xD8 (PCA Control 0)

PCA0CN0\_CCF0 BIT PCA0CN0.0 ; PCA Module 0 Capture/Compare Flag

PCA0CN0\_CCF1 BIT PCA0CN0.1 ; PCA Module 1 Capture/Compare Flag

PCA0CN0\_CCF2 BIT PCA0CN0.2 ; PCA Module 2 Capture/Compare Flag

PCA0CN0\_CR BIT PCA0CN0.6 ; PCA Counter/Timer Run Control

PCA0CN0\_CF BIT PCA0CN0.7 ; PCA Counter/Timer Overflow Flag

; PSW 0xD0 (Program Status Word)

PSW\_PARITY BIT PSW.0 ; Parity Flag

PSW\_F1 BIT PSW.1 ; User Flag 1

PSW\_OV BIT PSW.2 ; Overflow Flag

PSW\_RS0 BIT PSW.3 ; Register Bank Select Bit 0

PSW\_RS1 BIT PSW.4 ; Register Bank Select Bit 1

PSW\_F0 BIT PSW.5 ; User Flag 0

PSW\_AC BIT PSW.6 ; Auxiliary Carry Flag

PSW\_CY BIT PSW.7 ; Carry Flag

; SCON0 0x98 (UART0 Serial Port Control)

SCON0\_RI BIT SCON0.0 ; Receive Interrupt Flag

SCON0\_TI BIT SCON0.1 ; Transmit Interrupt Flag

SCON0\_RB8 BIT SCON0.2 ; Ninth Receive Bit

SCON0\_TB8 BIT SCON0.3 ; Ninth Transmission Bit

SCON0\_REN BIT SCON0.4 ; Receive Enable

SCON0\_MCE BIT SCON0.5 ; Multiprocessor Communication Enable

SCON0\_SMODE BIT SCON0.7 ; Serial Port 0 Operation Mode

; SMB0CN0 0xC0 (SMBus 0 Control)

SMB0CN0\_SI BIT SMB0CN0.0 ; SMBus Interrupt Flag

SMB0CN0\_ACK BIT SMB0CN0.1 ; SMBus Acknowledge

SMB0CN0\_ARBLOST BIT SMB0CN0.2 ; SMBus Arbitration Lost Indicator

SMB0CN0\_ACKRQ BIT SMB0CN0.3 ; SMBus Acknowledge Request

SMB0CN0\_STO BIT SMB0CN0.4 ; SMBus Stop Flag

SMB0CN0\_STA BIT SMB0CN0.5 ; SMBus Start Flag

SMB0CN0\_TXMODE BIT SMB0CN0.6 ; SMBus Transmit Mode Indicator

SMB0CN0\_MASTER BIT SMB0CN0.7 ; SMBus Master/Slave Indicator

; SPI0CN0 0xF8 (SPI0 Control)

SPI0CN0\_SPIEN BIT SPI0CN0.0 ; SPI0 Enable

SPI0CN0\_TXBMT BIT SPI0CN0.1 ; Transmit Buffer Empty

SPI0CN0\_NSSMD0 BIT SPI0CN0.2 ; Slave Select Mode Bit 0

SPI0CN0\_NSSMD1 BIT SPI0CN0.3 ; Slave Select Mode Bit 1

SPI0CN0\_RXOVRN BIT SPI0CN0.4 ; Receive Overrun Flag

SPI0CN0\_MODF BIT SPI0CN0.5 ; Mode Fault Flag

SPI0CN0\_WCOL BIT SPI0CN0.6 ; Write Collision Flag

SPI0CN0\_SPIF BIT SPI0CN0.7 ; SPI0 Interrupt Flag

; TCON 0x88 (Timer 0/1 Control)

TCON\_IT0 BIT TCON.0 ; Interrupt 0 Type Select

TCON\_IE0 BIT TCON.1 ; External Interrupt 0

TCON\_IT1 BIT TCON.2 ; Interrupt 1 Type Select

TCON\_IE1 BIT TCON.3 ; External Interrupt 1

TCON\_TR0 BIT TCON.4 ; Timer 0 Run Control

TCON\_TF0 BIT TCON.5 ; Timer 0 Overflow Flag

TCON\_TR1 BIT TCON.6 ; Timer 1 Run Control

TCON\_TF1 BIT TCON.7 ; Timer 1 Overflow Flag

; TMR2CN0 0xC8 (Timer 2 Control 0)

TMR2CN0\_T2XCLK0 BIT TMR2CN0.0 ; Timer 2 External Clock Select Bit 0

TMR2CN0\_T2XCLK1 BIT TMR2CN0.1 ; Timer 2 External Clock Select Bit 1

TMR2CN0\_TR2 BIT TMR2CN0.2 ; Timer 2 Run Control

TMR2CN0\_T2SPLIT BIT TMR2CN0.3 ; Timer 2 Split Mode Enable

TMR2CN0\_TF2CEN BIT TMR2CN0.4 ; Timer 2 Capture Enable

TMR2CN0\_TF2LEN BIT TMR2CN0.5 ; Timer 2 Low Byte Interrupt Enable

TMR2CN0\_TF2L BIT TMR2CN0.6 ; Timer 2 Low Byte Overflow Flag

TMR2CN0\_TF2H BIT TMR2CN0.7 ; Timer 2 High Byte Overflow Flag

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; Interrupt Definitions

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INT0\_IRQn EQU 0 ; External Interrupt 0

TIMER0\_IRQn EQU 1 ; Timer 0 Overflow

INT1\_IRQn EQU 2 ; External Interrupt 1

TIMER1\_IRQn EQU 3 ; Timer 1 Overflow

UART0\_IRQn EQU 4 ; UART 0

TIMER2\_IRQn EQU 5 ; Timer 2 Overflow

SPI0\_IRQn EQU 6 ; SPI0

SMBUS0\_IRQn EQU 7 ; SMBus 0

RTC0ALARM\_IRQn EQU 8 ; RTC0 Alarm

ADC0WC\_IRQn EQU 9 ; ADC0 Window Compare

ADC0EOC\_IRQn EQU 10 ; ADC0 End of Conversion

PCA0\_IRQn EQU 11 ; PCA0

CMP0\_IRQn EQU 12 ; Comparator 0

TIMER3\_IRQn EQU 14 ; Timer 3 Overflow

VDDMON\_IRQn EQU 15 ; Supply Monitor Early Warning

PMATCH\_IRQn EQU 16 ; Port Match

RTC0FAIL\_IRQn EQU 17 ; RTC0 Oscillator Fail

CS0EOC\_IRQn EQU 19 ; CS0 End of Conversion

CS0DCMP\_IRQn EQU 20 ; CS0 Digital Comparator

CS0EOS\_IRQn EQU 21 ; CS0 End of Scan

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; SFR Page Definitions

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LEGACY\_PAGE EQU 000H ; Legacy SFR Page

CONFIG\_PAGE EQU 00FH ; System and Port Configuration Page

CRC0\_PAGE EQU 00FH ; CRC0 Page

TOFF\_PAGE EQU 00FH ; Temperature Sensor Calibration Offset Page